CIRCUITS PROCESSING TECHNOLOGY INC.

1817 Peacock Blvd., Oceanside, CA 92056

Dated: 1-22-03
Drawing L2S Stereo

1D Team Members:

Zan Aslett, Director of Operations
Clark Steddom, Engineering Manager
Dave Pivic, Sales Manager
Josh Habib, Quality Manager

2D Description of Issue from Customer:

Two parts have the clock line open at the same point on both boards.

3D Containment Actions:

There are no completed parts at CPT.

4D Analysis Procedure and Results:

The two parts returned with the opens were examined visually and electrically tested to confirm the opens. The method of test (Teledyne Tac) was confirmed to be able to detect the opens. The two boards were reworked to correct the open clock net and verified to be correct. The two boards were not completely retested with the Teledyne Tac or the Probot tester. The two corrected boards were returned.

5D Identification of Root Cause:

A closed via was found between the top metal and the adjacent underlying metal. It was the same via on both boards. The depth of the dielectric blocking the via stack indicated that the emulsion had been lost from the screen during the printing of the second to the last coat of dielectric before the top metal.

6D Identification of Improvement:

Closed vias in the thick film technology are always possibilities. We use visual inspection methods to reduce the potential of closed vias. All these inspections were in place. The larger the board and the greater the number of vias reduces the possibility of catching closures with visual inspection. We use electrical test methods (Teledyne Tac) at each metal layer to find circuit problems. These electrical test methods were in place. We have determined that the two open circuits were true test escapes due to operator error. We recently purchased a new electrical tester that uses true isolation continuity methods for test rather than the single point capacitance probe method of the Teledyne Tac. The new tester (Probot) is programmed from the gerber files that generate the artwork used to build the boards and when an error occurs it identifies the exact location of the circuit problem. The single point prober is manually programmed and is subject to program error and does not directly identify the problem location.

7D Implementation of Improvement:

The new Probot tester was just recently purchased and implemented. A new test engineer was added to the staff to support the test operation. The lot of boards that had the errors were shipped prior to completion of the implementation of the new tester.

8D Preventive Action:

The preventative action will be to use the new tester for final acceptance of multilayer product that we build. There are two more lots of boards (Axiel and Stereo) that are in work to complete the current order. Both these lots will use the new Probot tester for their final acceptance.

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Josh Habib
QA. Manager